

REMARKS

The specification has been amended on page 1 to complete the citations of the prior applications.

The claims have been amended to more clearly define the invention as disclosed in the written description. In particular, claims 1, 15, 18, 22 and 25 have been amended for clarity.

The Examiner has rejected claims 1, 4, 5, 7, 8, 11, 12, 14, 15, 18, 19 and 23-25 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0028076 to Strolle et al. in view of U.S. Patent Application Publication No. 2002/0191712 to Gaddam et al. In addition, the Examiner has rejected claims 2, 9 and 16 under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. in view of Gaddam et al., and further in view of U.S. Patent 6,034,731 to Hurst, Jr. Furthermore, the Examiner has rejected claims 6, 13 and 20 under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. in view of Gaddam et al., and further in view of U.S. Patent Application Publication No. 2001/0055342 to Fimoff. The Examiner has moreover rejected claims 22 and 27 under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. in view of U.S. Patent 6,621,527 to Limberg et al. Finally, the Examiner has rejected claims 23-25 under 35 U.S.C. 103(a) as being unpatentable over Strolle et al. in view of Gaddam et al., and further in view of U.S. Patent Application Publication No. 2003/0099303 to Birru et al.

The Strolle et al. publication discloses a bitstream that includes normal packets and robust packets. Strolle et al. also

discloses that when a standard Reed-Solomon encoder is employed to generate the normal packets, then the parity bytes are output at the end of the decoded normal packets generated by a corresponding Reed-Solomon encoder. Strolle et al. also discloses that when a non-standard Reed-Solomon encoder is employed to generate the robust packets, then the parity bytes in the robust packets are relocated so that the parity bytes all come out of the corresponding non-standard Reed-Solomon decoder first for the decoded robust packets (see paragraphs [0061]-[0063]).

Strolle et al. also discloses that the locations of the robust packets and the normal packets within a frame are known by reference to a robust mode tier control code value which is communicated to the receiver (see paragraph [0049]).

Strolle et al. further discloses that, at the receiver, the non-standard Reed-Solomon decoder must reorder the bytes for each packet depending on whether it is a robust packet or a normal packet, which can be determined from where the packet is located in the frame (using the robust mode tier control code value) (see paragraphs [0083]-[0084]).

It is evident from the above description that in Strolle et al., the locations of the parity bytes in the robust packets are different than the locations of the parity bytes in the normal packets. However, the locations of the parity bytes in all of the robust packets are the same as each other so that the parity bytes for each robust packet always come out of the non-standard Reed-Solomon decoder first.

Therefore, Applicants respectfully submit Strolle et al. does not disclose a second processor block for determining the locations of the parity bytes of a robust packet according to the robust packet's position within the frame. Indeed, as explained above, Applicants respectfully submit that Strolle et al. teaches that the locations of the parity bytes within each robust packet are the same as each other regardless of the robust packet's position within the frame.

Also among other things, the packet formatter of Claim 1 includes a third processing block for receiving a first output signal and removing therefrom duplicate bits associated with the robust stream to thereby produce a second output signal that is output from a data path output of the packet formatter.

The Gaddam et al. publication discloses a packet identification mechanism at the transmitter and receiver for an enhanced ATSC 8-VSB system.

The Examiner now indicates that Gaddam et al. discloses "that the locations of the parity bytes a robust packet being dependent upon a position of the robust packet within a frame of the robust packets and standard packets in the dual bit stream signal and a second processing block capable of determining the locations of the parity bytes within the robust packet according to the robust packet's position within the frame and a third processing block capable of receiving said first output signal and removing therefrom duplicate bits associated with said robust

stream to thereby produce a second output signal that is output from a data path output of said packet formatter" and states:

"paragraphs 0066-0068 the transmitter encodes the MODE, NRS, NRP, and RPP information into the stream in order for the receiver to properly decode both bit streams; the receiver extracts and uses the four control parameters to determine the location of the robust the dual bit-stream; paragraph 0057 further discloses that if NRS=1 (i.e., non-systematic RS-encoding is employed for backwards compatibility at existing receiver devices) then, the packet formatter (at the transmitter) additionally inserts 'place holders' for the additional header and parity bytes; with the control parameters the receiver can locate and identify the additional header and parity bytes; Paragraph 0054 further discloses for robust streams, the information bit need only be placed in the robust byte at the desirable bit position for robust trellis encoding and symbol mapping. With greater particularity, at the MPEG packet level, for each robust packet carrying information, two packets are generated: one being the information carrier packet, and the other functioning as a placeholder packet. In the packet formatter 330, only the information carrier packet (not the placeholder packet) is processed. Particularly as shown in FIG. 6, the packet formatter generates two robust bytes (packets) 332a, 332b for each byte 331 of each packet received from the robust stream. The packet formatter 330 will generate two identical bits, e.g., bits 333, 334 corresponding to each information bit 335 of each input byte processed; Paragraph 0068 further discloses the Packet Formatter block 555 reformats the robust bit-stream packets. When NRS=0, it transforms two NS packets into one packet for input to the RS decoder block 560]."

Applicants submit that the Examiner is misreading Gaddam et al. In particular, the Examiner states "paragraphs 0066-0068 the transmitter encodes the MODE, NRS, NRP, and RPP information into the stream in order for the receiver to properly decode both bit streams; the receiver extracts and uses the four control parameters to determine the location of the robust the dual bit-stream". However, Gaddam et al., at paragraphs [0066]-[0068], states:

"**[0066]** Referring back to FIG. 3, as the receiver needs MODE, NRS, NRP and RPP information in order for it to properly decode both the bit-streams, the parameters themselves have to be robustly encoded so that they can be decoded even in severe multi-path channels. The encode sync header block 360 performs this function and, after encoding, the encode sync header block 360 places the encoded code-word in a fixed location (reserved bits) in the Frame Sync segment 370. These control parameters are extracted from the detected frame synch signal at the receiver device. The output of the trellis encoder 350, and frame synch signal 370 including the encoded control parameters is then multiplexed by multiplexor unit 365 to form a multiplexed signal 380 which is subject to the pilot insertion and RF up-conversion (FIG. 1).

"**[0067]** FIG. 10 illustrates a block diagram of a novel ATSC receiver 500 capable of decoding both the standard and new (robust) bit-streams. The embodiment of the receiver 500 depicted in FIG. 10 exemplifies the case when non-systematic RS encoder is not used, i.e., the control parameter NRS=0. As in the transmission system of FIG. 3, the receiver device 500 is provided for decoding the two types of bit streams and, particularly employs an extensive control mechanism 550 to properly track the symbols (bytes) belonging to the two symbol streams. It also implements a packet formatter to reformat the new (robust) NS packets.

"**[0068]** As shown in FIG. 10, after carrier demodulation and received signal equalization 502 are performed, a sync detect block 505 detects the frame sync signal present in the received signal 370' that includes the encoded control parameter information associated with the received packets. A Decode sync header block 510 is provided to decode the Frame Sync header information and extract the MODE, NRS, NRP and RPP control parameters. These parameters are then sent to a 'Generate hd_sd_in' block 515 and 'Generate ps_hd_sd' block 520. Particularly, as shown in FIG. 10, the Generate 'hd_sd_in' block 515 generates control information at packet level based on MODE, NRP and RPP parameters. For example, the output of this block is equal to '1' if the packet belongs to NS (new stream) and is equal to '0' if the packet belongs to SS (standard stream). This block only starts when a back-end lock (not shown) is obtained. The Generate 'ps_hd_sd' block 520 is similar to the Generate 'hd_sd_in' block 515 except that it is synchronized with the de-interleaver output sync and start up signals when the de-interleaver output start signal (not shown) toggles high. The Convolutional bit

interleaver block 520 is similar to convolutional byte interleaver specified in the ATSC standard, except that the memory element is 1 bit instead of 1 byte. This block 520 is used to track bytes through the convolutional de-interleaver 540. Likewise, the Trellis interleaver block 525 implements the 12-symbol trellis interleaver. The output of this block 'td hd sd' signal 526 will be greater than 0 (e.g., 1 for H-VSB, 2 for 4-VSB or 3 for pseudo 2-VSB) when the trellis decoder input symbol (or equalizer output symbol) 390 belongs to NS and is equal to 0 when the trellis decoder input symbol 390 belongs to SS. Functionally, the blocks 515, 520 and 525 in the receiver are similar to the corresponding blocks 315, 341 and 345 in the transmitter. The equalizer 502 additionally uses this signal 526 to get a better estimate of the symbol and the trellis decoder 530 uses this signal in metric calculation. The Packet Formatter block 555 reformats the robust bitstream packets. When NRS=0, it transforms two NS packets into one packet for input to the RS decoder block 560."

Applicants submit that it should be apparent from the above that while Gaddam et al. discloses the encoding, transmission, reception, decoding and processing of the control parameters MODE, NRS, NRP and RPP, there is no disclosure that Gaddam et al. uses these parameters to determine "the locations of the parity bytes within each robust packet according to the robust packet's position within the frame".

The Examiner then states "paragraph 0057 further discloses that if NRS=1 (i.e., non-systematic RS-encoding is employed for backwards compatibility at existing receiver devices) then, the packet formatter (at the transmitter) additionally inserts 'placeholders' for the additional header and parity bytes; with the control parameters the receiver can locate and identify the additional header and parity bytes".

Applicants submit that while Gaddam et al. indicates that "place holder" are inserted for the additional header and parity bytes, it should be clear that the packet formatter of Gaddam et al. is at the transmission end for forming the dual bitstream signal, and that Gaddam et al. neither discloses nor suggests "a second processing block for determining the locations of the parity bytes within each robust packet according to the robust packet's position within the frame, said first processing block, in response to the determined locations of the parity bytes within each robust packet, removing the header bytes and parity bytes from the dual bitstream signal to output a first output signal".

Claim 2 claims "The packet formatter as set forth in claim 1 wherein said packet formatter passes bytes associated with said standard stream to said data path output of said packet formatter after delaying said standard stream bytes by a predetermined delay time."

The Hurst, Jr. patent discloses an MPEG frame processing method and apparatus.

The Examiner states that Hurst, Jr. discloses this limitation at col. 4, lines 1-5 "the MPEG picture header has contains a delay number that indicates the amount of time a decoder should wait until it decodes the picture".

Applicants submit while Hurst, Jr. discloses the amount of time a decoder should wait until it decodes the picture, Hurst, Jr. neither discloses nor suggests that the packet formatter should

pass bytes associated with the standard stream (as opposed to processing these bytes along with the bytes of the robust stream), and that these passed bytes should be delayed.

Applicants further submit that Hurst, Jr. does not supply that which is missing from Strolle et al. and Gaddam et al., as noted above.

Claim 6 claims "The packet formatter as set forth in claim 5 wherein said packet formatter generates and outputs packet identification information used by subsequent processing blocks following said packet formatter."

The Fimoff publication discloses a mapping arrangement for digital communication system.

The Examiner states that Fimoff discloses this limitation at para. [0043], lines 1-7 "the Decoder 50 decodes the stream of data which includes packet identifications (PID's) and based on the PID's the RVSB receiver either discards or forwards the data to outer decoder 56; therefore the Decoder regenerates the PID from the coded data stream".

Applicants believe that the Examiner is mis-reading Fimoff. In particular, the noted section of Fimoff states: "The output of the 2/3 rate inner decoder 50 is deinterleaved by a deinterleaver 52. The robust VSB receiver 14 reads the PID's of all packets at the output of the deinterleaver 52. Based upon these PID's, the robust VSB receiver 14 discards those packets at 54 which have the PID's of ATSC data and also discards the transport

headers added following the outer coder 20 and the parity bytes added by the Reed-Solomon encoder 28." Hence, there is no disclosure that the "packet formatter generates and outputs packet identification information used by subsequent processing blocks following said packet formatter" as specifically set forth in claim 6.

Further, Applicants submit that Fimoff does not supply that which is missing from Strolle et al. and Gaddam et al., as set forth above.

Claim 22 claims "A data de-randomizer for use in a television receiver capable of receiving a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream, said data de-randomizer comprising:

a standard de-randomizer for de-randomizing bytes associated with said standard stream; and

a robust de-randomizer for de-randomizing bytes associated with said robust stream,

wherein said data de-randomizer further comprises a delay calculation circuit for determining a delay associated with the robust stream with respect to a field synchronization signal, and applying a control signal to the robust de-randomizer to cause the robust de-randomizer to suspend its operation for a portion of a field in accordance with the determined delay."

The Examiner has indicated that Strolle et al. discloses the data de-randomizer (De-randomizer 334 in Fig. 3A) which comprises a standard de-randomizer and a robust de-randomizer ("the VSB De-randomizer is operates on both the normal and robust bytes"). The Examiner then states "Strolle et al. does not disclose that the data derandomizer further comprises a delay calculation circuit for determining a delay with respect to a field synchronization signal associated with the robust stream and applying a control signal to the robust de-randomizer to cause the robust de-randomizer to suspend id [sic] operation for a portion of a field in accordance with the determined delay. However, Limberg et al. discloses such a feature (column 6, lines 21-22 [the delay circuit provides a delay which is adjustable in response to a control signal]))."

Applicants submit that the Examiner is mistaken. In particular, Limberg et al. states, at col. 6, lines 19-22, "This third IF signal response is the final intermediate-frequency output signal of the tuner 5, which is supplied to an analog delay circuit 22, the delay through which his adjustable in response to an electrical control signal." Quite obviously, an analog delay circuit cannot be used in the digital arrangement of Strolle et al.

Further, claim 22 claims "a delay calculation circuit for determining a delay associated with the robust stream with respect to a field synchronization signal, and applying a control signal to the robust de-randomizer to cause the robust de-randomizer to suspend its operation for a portion of a field in accordance with

the determined delay." As clearly set forth in Limberg et al. the analog delay circuit's delay is determined by a control signal, and does not generate any control signal.

In addition, there is no disclosure or suggestion in Strolle et al. nor Limberg et al. how the VSB derandomizer is to be configured such that a control signal is applied thereto to only delay de-randomizing the robust stream.

Claim 23 claims "The packet formatter of claim 1, wherein locations of the parity bytes within a first one of the robust packets within the frame are different than locations of the parity bytes within a second one of the robust packets within the frame, and wherein the second processing block is capable of determining the locations of the parity bytes within each of the first and second robust packets according to the first and second robust packets' corresponding positions within the frame."

The Birru et al. publication discloses a digital television (DTV) transmission system using enhanced coding schemes. Applicants submit, however, that Birru et al. does not supply that which is missing from Strolle et al. and Gaddam et al., as set forth above.

In view of the above, Applicants believe the subject invention, as claimed, is not rendered obvious by the prior art, either individually or collectively, and as such, is patentable thereover.

Applicants believe that this application, containing claims 1, 2, 4-9, 11-13, 15, 16, 18-20 and 22-27, is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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